REMARKS

Reconsideration is respectfully requested.

The presently pending Claims 1-3, 5, 6 and 8-9 have been rejected under 35 U.S. C. §103(a) over the applicants' description of the prior art ("AAPA"), as set forth and illustrated in Figs. 1 and 2 of this application, in view of Maniar et al. (U.S. Pat. No. 5,356,833).

Applicants continue to respectfully submit that the AAPA does not teach the claimed invention, as is explained in the specification at pages 1-6, and in view of the arguments made below. Moreover, neither do Maniar et al. provide any teaching that, either together with or separately from AAPA, there is any combination that can properly support the rejection. In fact, Maniar et al. teach away from making the proposed combination.

The Examiner is thanked for his time and the courtesies extended during the telephone conversation of October 15, 2003, in explanation of the rejection set forth in the Office Action. The Examiner's explanation in effect more clearly provides the basis for the rejection, which, as understood, is that using the structural gate as embodied at the step in Fig. 2, the teaching of Maniar et al. is utilized to modify the structure in order to obtain the MOSFET semiconductor recited in the claims of this application.

Applicants again rely on the arguments made in the Amendment entered July 21, 2003, in view of the further explanation made below, but do not set forth those arguments herein so as to avoid repetition thereof.

Additional reasons are present that mandate a finding of non-obviousness of the claimed invention. The specification relating to the embodiment shown in Fig. 2 of the present application described certain problems generated from a method of forming a gate in a semiconductor device using a conventional process. The conventional method teaches that the

CMP process be carried out along the dotted line AA' to provide complete planarization, without a wave-like structure. Further, as explained below, in the conventional method, the CMP process is carried out non-selectively between the insulating interlayer and the dummy gate polysilicon layer. Therefore, upon considering such a planarization effect and non-selective polishing as used in conventional CMP process, it is well understood that a linear top profile of metal gates is formed from the conventional method in accordance with the prior art shown in Fig. 2.

The rejection of the claims further relies on Maniar et al. as disclosing the use of CeO_2 slurry for providing the CMP oxide removal, and while it may be true that use of the material CeO_2 is well known a slurry for CMP polishing, there is no teaching in Maniar et al. or any other cited reference using "a metal CMP process utilizing a second high selection ratio sufficient to polish the metal layer but insufficient to polish the insulating interlayer, wherein the second high selection ratio between the insulating interlayer and the gate metal layers is over 50," as recited in Claim 1.

In the present invention, polishing between the insulating layer and the dummy gate polysilicon layer and between the insulating interlayer and the gate metal layer is selectively carried out, more particularly, the polishing selection ratios of the insulating interlayer to the dummy gate polysilicon layer and of the gate metal layer to insulating interlayer are high, particularly over 20 and 50, respectively to achieve the "wave-like" profile shown in Fig. 3F. This contrasts directly with the teaching of Maniar et al., wherein it is described that "A polishing step should have a selectivity as close to 1:1 (polishing rate of the AB_3 layer to the polishing rate of the insulating layer) as possible because of AB_3's expected resistance to attack by many chemicals. (...) Because a relatively non-selective polishing method would be used, the abrasive particles will usually be alumina or cerium dioxide" (emphasis added) (see column

5, lines 53-63 of the Maniar et al. reference). Therefore, Maniar et al. fails to teach or suggest any motivation or incentive to select the high polishing selection ratios, as recited in Claim 1 of the present invention, and the indication in the Office Action, page 2 that because the same slurry material is used "in the same CMP step to have the same selective ratio between the insulating layer and the gate metal layer" is not only not taught by Maniar et al., but is in fact taught against by that reference. Reliance on Maniar et al. is thus considered misplaced and improper.

The presently claimed inventive method produces metal gates having a non-linear (wave-like) top profile, which solves the problems caused by the conventional method of forming a gate (see column 2, paragraph 18 of the published application; last paragraph of Page 5 of the specification). Use of this method achieves favorable results, such as reduction of height of the dummy gate polysilicon layer, and the insulating layer being deposited between the gates without voids due to the short dummy gate, etc. (see columns 5-6, numbered paragraphs 45-46 of the published application; last paragraph of Page 13 to page 14, line 11 of the specification).

With respect to the indication in the Office Action that the "wave-like" profile will be inherently produced if the materials of the AAPA (Fig. 2) are used with the material described by Maniar et al., it is respectfully suggested that the "wave-like" profile cannot be formed due to the use in a conventional process, such as that shown in Figs. 1 and 2, of a conventional CMP process on the insulation interlayer 7, see page 4, lines 12-14, which process produces complete planarization of the entire surface along the line AA', as shown in Fig. 2 and as described above. Moreover, Maniar et al. cannot be relied on for teaching a modification of the conventional method, because Maniar et al. teach away from such a modification, since Manair et al. teaches a non-selective polishing method and a selectivity ratio of 1:1 (not 50:1, as is recited in Claim 1), see above. That is, because Maniar et al. also teach a complete planarization of the surface, see Column 5, lines 49-53 and Figs. 10-11 of

Maniar et al. Thus, not only is there no incentive taught for the modification, but such a modification is taught away from, as described in Maniar et al. Accordingly, the indication in the Office Action that the "wave-like" profile would simply result from a simple change of the chemical polishing material to CeO_2 is improper. Thus it is respectfully suggested that the rejection based on AAPA, as modified by the teachings of Maniar et al., is also improper.

In view of the above, moreover, the suggestion made in the rejection that it would be obvious to combine the teaching of Maniar et al. as teaching a CMP process using high etch selectivity does not provide the requisite teaching of using such a high selectivity etch in the process described in the Admitted Prior Art. The only such teaching is found in the present invention, as described in the specification and as recited in Claim 1, but reliance on such a teaching in an obviousness rejection is respectfully submitted as being impermissible hindsight reasoning.

Therefore the present invention as claimed in Claim 1 is non-obvious over AAPA in view of the lack of a proper teaching of US Patent No. 5,356,833 to Maniar et al. that it is combinable with AAPA. Claims 2-3, 5-6 and 8-9, because of their dependency on Claim 1, are also considered to be patentable.

For the above reasons, Applicants respectfully request reconsideration and withdrawal of the outstanding rejections. An indication of allowable subject matter is earnestly solicited.

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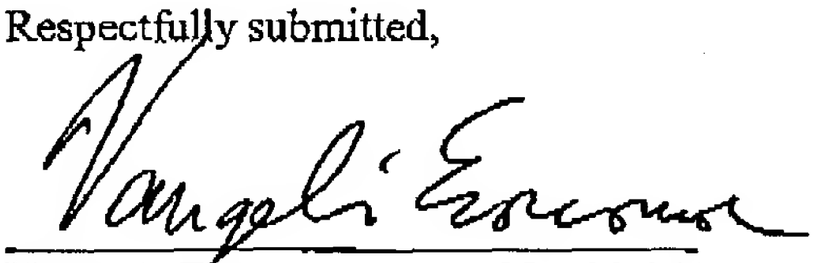
Respectfully submitted,



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